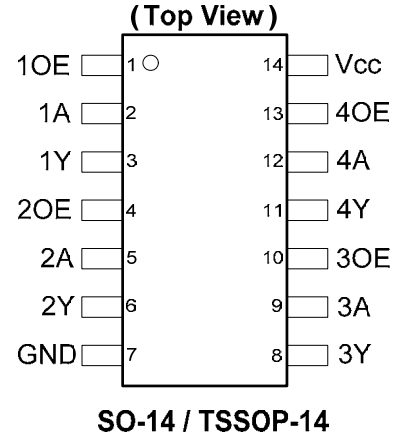


Description

The 74LVC126A provides four independent buffers with three state outputs. Each output is independently controlled by an associated output enable pin (OE) which places the device in the high impedance state when driven low. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output preventing damaging current backflow when the device is powered down.

Pin Assignments



SO-14 is a future product

Features

- Supply Voltage Range from 1.65V to 5.5V
- Sinks 24mA at $V_{CC} = 3.3V$
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs or outputs accept up to 5.5V
- Inputs can be driven by 3.3V or 5.5V allowing for voltage translation applications.
- ESD Protection Exceeds JESD 22
 - 200-V Machine Model (A115-A)
 - 2000-V Human Body Model (A114-A)
 - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- Range of Package Options
- SO-14^{††} and TSSOP-14 Available in “Green” Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Applications

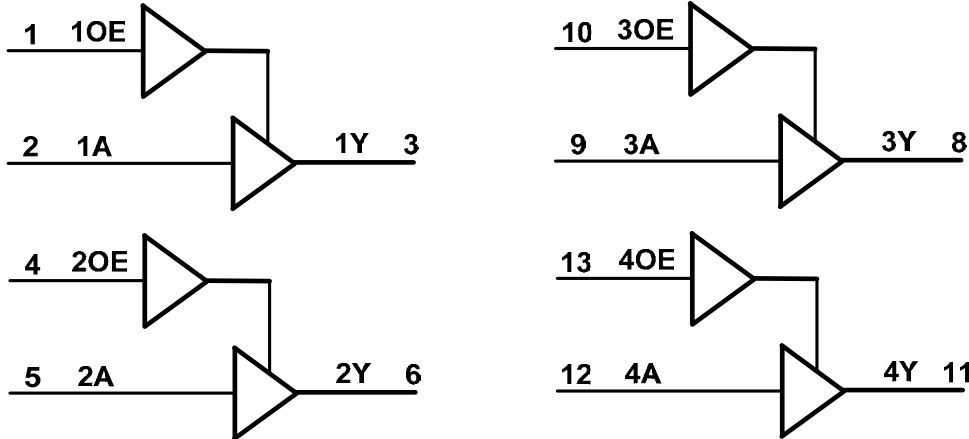
- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide array of products such as:
 - PCs, networking, notebooks, ultrabooks, netbooks
 - Computer peripherals, hard drives, CD/DVD ROM
 - TV, DVD, DVR, set top box

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

Pin Descriptions

Pin Number	Pin Name	Description
1	1OE	Data Enable Input (active high)
2	1A	Data Input
3	1Y	Data Output
4	2OE	Data Enable Input (active high)
5	2A	Data Input
6	2Y	Data Output
7	GND	Ground
8	3Y	Data Output
9	3A	Data Input
10	3OE	Data Enable Input (active high)
11	4Y	Data Output
12	4A	Data Input
13	4OE	Data Enable Input (active high)
14	V _{CC}	Supply Voltage

Logic Diagram



Function Table

Inputs		Output
OE	A	Y
H	H	H
H	L	L
L	X	Z

Absolute Maximum Ratings (Note 2)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD CDM	Charged Device Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	Supply Voltage Range	-0.5 to 6.5	V
V_I	Input Voltage Range	-0.5 to 6.5	V
V_O	Voltage applied to output in high impedance or I_{OFF} state	-0.5 to 6.5	V
V_O	Voltage applied to output in high or low state	-0.3 to $V_{CC} + 0.5$	V
I_{IK}	Input Clamp Current $V_I < 0$	-50	mA
I_{OK}	Output Clamp Current $V_O < 0$	-50	mA
I_O	Continuous output current	± 50	mA
I_{CC}, I_{GND}	Continuous current through V_{CC} or GND	± 100	mA
T_J	Operating Junction Temperature	-40 to 150	$^{\circ}C$
T_{STG}	Storage Temperature	-65 to 150	$^{\circ}C$
P_{TOT}	Total Power Dissipation	500	mW

Notes: 2. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	Active Mode	0	V_{CC}	V
		$V_{CC} = 0V$; Power Down Mode	0	5.5	V
$\Delta t/\Delta V$	Input transition rise or fall rate	$V_{CC} = 1.65V$ to $2.7V$		20	ns/V
		$V_{CC} = 2.7V$ to $3.6V$		10	
T_A	Operating free-air temperature		-40	125	$^{\circ}C$

Notes: 3. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics

Symbol	Parameter	Test Conditions	V _{CC}	T _A = -40°C to 85°C		T _A = -40°C to 125°C		Unit
				Min	Max	Min	Max	
V _{IH}	High-level Input Voltage		1.65V to 1.95V	0.65 X V _{CC}		0.65 X V _{CC}		V
			2.3V to 2.7V	1.7		1.6		
			2.7V to 3.6V	2.0		2.0		
V _{IL}	Low-level input voltage		1.65V to 1.95V		0.35 X V _{CC}		0.35 X V _{CC}	V
			2.3V to 2.7V		0.7		0.7	
			2.7V to 3.6V		0.8		0.8	
V _{OH}	High Level Output Voltage	I _{OH} = -100 μA	1.65V to 3.6V	V _{CC} - 0.2		V _{CC} - 0.3		V
		I _{OH} = -4 mA	1.65V	1.2				
		I _{OH} = -8 mA	2.3V	1.9				
		I _{OH} = -12 mA	2.7V	2.2		2.05		
		I _{OH} = -24 mA	3.0V	2.3		2.1		
V _{OL}	High-level Output Voltage	I _{OH} = 100 μA	1.65V to 3.6V		0.2		0.3	V
		I _{OH} = 4 mA	1.65V		0.45		0.6	
		I _{OH} = 8 mA	2.3V		0.70		0.85	
		I _{OH} = 12 mA	2.7V		0.40		0.6	
			3.0V		0.55		0.6	
		I _{OH} = -24 mA	3.0V		0.55		0.6	
I _I	Input Current	V _I = GND to 5.5V	3.6V		± 5		± 20	μA
I _{OZ}	Z State Leakage Current	V _O = GND or 5.5V	3.6V		± 10		± 20	μA
I _{OFF}	Power Down Leakage Current	V _I or V _O = 0V to 3.6V	0		10		20	μA
I _{CC}	Supply Current	V _I = GND or V _{CC} I _O = 0	3.6V		10		40	μA
ΔI _{CC}	Additional Supply Current	One input at V _{CC} - 0.6V Other	2.7V to 3.6V		500		5000	μA

Switching Characteristics

Parameter	From (Input)	To (Output)	Test Conditions See Figure 1	25°C			-40°C to 85°C		-40°C to 125°C		Unit
				Min	Typ.	Max	Min	Max	Min	Max	
t_{pd}	A	Y	$V_{CC} = 1.8V \pm 0.15V$	1.0	4.2	9.3	1.0	9.8	1.0	11.3	ns
			$V_{CC} = 2.5V \pm 0.2V$	1.0	2.7	6.7	1.0	7.2	1.0	9.3	
			$V_{CC} = 2.7V$	1.0	2.9	5.0	1.0	5.2	1.0	6.5	
			$V_{CC} = 3.3V \pm 0.3V$	1.0	2.5	4.5	1.0	4.7	1.0	6.0	
t_{en}	OE	Y	$V_{CC} = 1.8V \pm 0.15V$	1.0	4.8	9.5	1.0	10	1.0	11.5	ns
			$V_{CC} = 2.5V \pm 0.2V$	1.0	2.1	7.8	1.0	8.3	1.0	10.4	
			$V_{CC} = 2.7V$	1.0	2.3	6.1	1.0	6.3	1.0	8.0	
			$V_{CC} = 3.3V \pm 0.3V$	1.0	2.5	5.5	1.0	5.7	1.0	7.5	
t_{dis}	OE	Y	$V_{CC} = 1.8V \pm 0.15V$	1.0	4.4	12.1	1.0	12.5	1.0	14.1	ns
			$V_{CC} = 2.5V \pm 0.2V$	1.0	2.7	8.2	1.0	8.7	1.0	10.8	
			$V_{CC} = 2.7V$	1.0	2.7	6.5	1.0	6.7	1.0	8.5	
			$V_{CC} = 3.3V \pm 0.3V$	1.0	2.3	5.8	1.0	6.0	1.0	7.5	
$t_{SK(0)}$			$V_{CC} = 3.3V \pm 0.3V$			1.0		1.0		1.5	ns

Operating Characteristics

$T_A = 25\text{ }^\circ\text{C}$

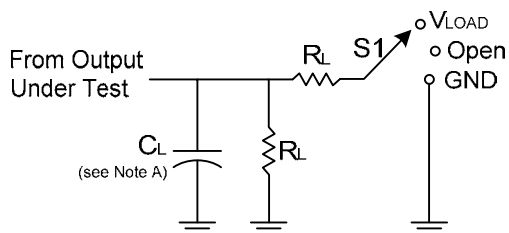
Parameter		Test Conditions	$V_{CC} = 1.8\text{V}$	$V_{CC} = 2.5\text{V}$	$V_{CC} = 3.3\text{V}$	Unit
			Typ.	Typ.	Typ.	
C_{pd}	Power dissipation capacitance per gate	$f = 10\text{ MHz}$	7.3	11.2	14.9	pF
C_i	Input Capacitance	$V_i = V_{CC} - \text{or GND}$	4	4	4	pF

Package Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	Min	Typ.	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	SO-14 ^{††}	(Note 4)		TBD		$^\circ\text{C/W}$
		TSSOP-14		159			
θ_{JC}	Thermal Resistance Junction-to-Case	SO-14 ^{††}	(Note 4)		TBD		$^\circ\text{C/W}$
		TSSOP-14		25			

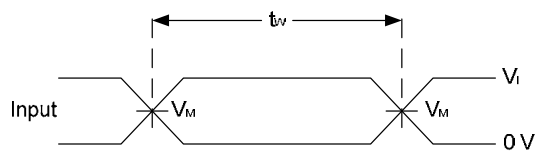
Notes: 4. Test condition for SO-14^{††} and TSSOP-14 : Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Parameter Measurement Information

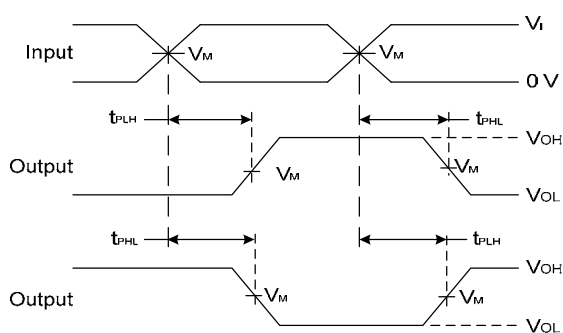


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

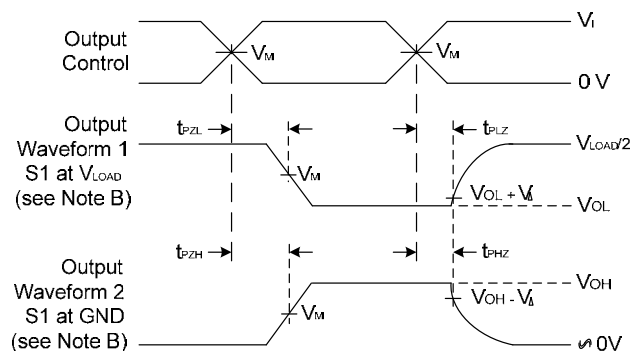
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1K Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
2.7V	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

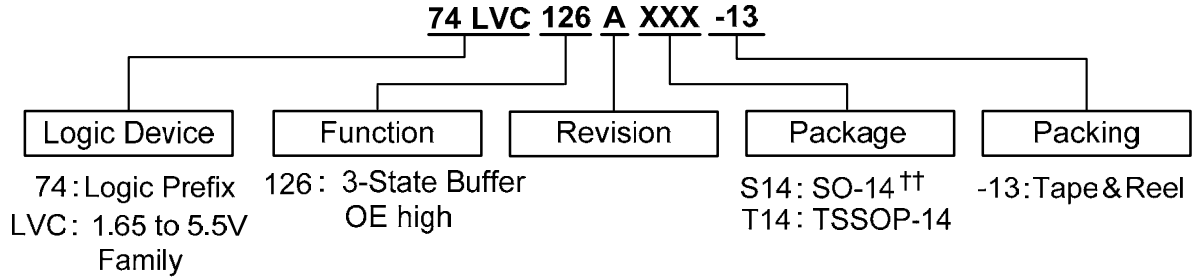


Voltage Waveform Enable and Disable Times Low and High Level Enabling

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
 - C. Inputs are measured separately one transition per measurement.
 - D. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - E. t_{PZL} and t_{PZH} are the same as t_{EN0} .
 - F. t_{PLH} and t_{PHL} are the same as t_{PD} .

Figure 1. Load Circuit and Voltage Waveforms

Ordering Information



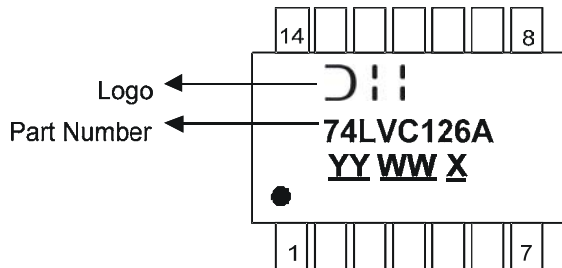
Device	Package Code	Packaging (Note 5)	13" Tape and Reel	
			Quantity	Part Number Suffix
74LVC126AS14-13	S14	SO-14 ^{††}	2500/Tape & Reel	-13
74LVC126AT14-13	T14	TSSOP-14	2500/Tape & Reel	-13



Notes: 5. The taping orientation and tape details can be found at <http://www.diodes.com/datasheets/ap02007.pdf>

Marking Information

(1) SO-14^{††} , TSSOP-14

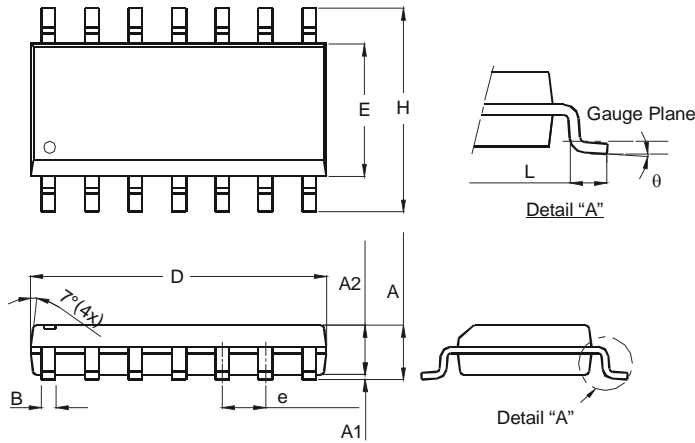


YY : Year : 08, 09, 10~
WW : Week : 01~52; 52 represents 52 and 53 week
X : Internal Code

Part Number	Package
74LVC126AS14	SO-14 ^{††}
74LVC126AT14	TSSOP-14

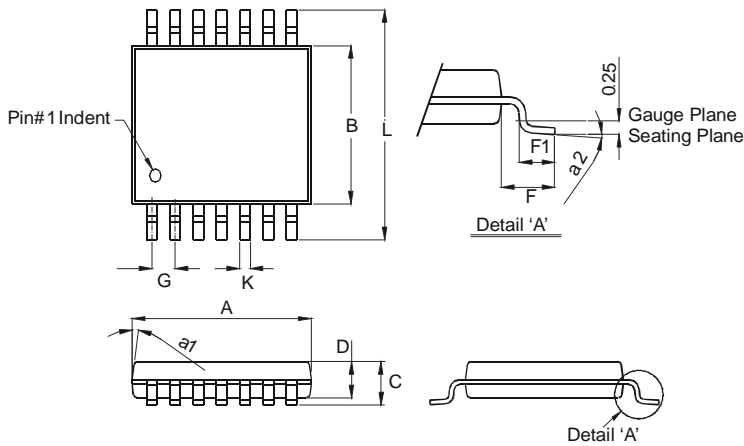
Package Outline Dimensions (All Dimensions in mm)

Package Type: SO-14^{††}



SO-14 ^{††}		
Dim	Min	Max
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

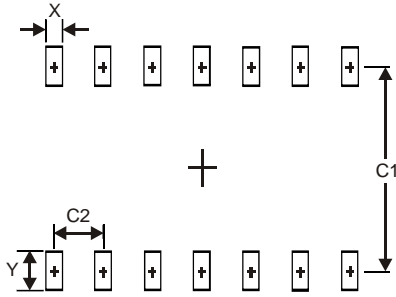
Package Type: TSSOP-14



TSSOP-14		
Dim	Min	Max
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

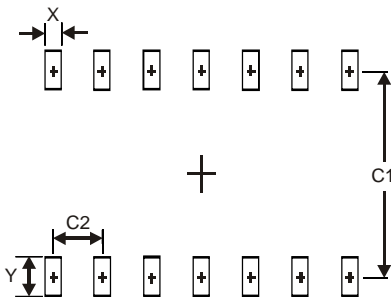
Suggested Pad Layout

Package Type: SO-14††



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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